# 53A-425 QUAD ARINC-429 TRANSMITTER CARD

# OPERATING MANUAL



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## OPERATING MANUAL

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## DESCRIPTION

The 53A-425 Quad ARINC-429 Transmitter Card is a printed circuit board assembly for use in a CDS 53/63 Series System. The card transmits data onto the Mark 33 Digital Information Transfer System (DITS) found on commercial aircraft. The 53A-425 Card has four independent transmitters, each with an associated buffer memory for storing up to 32,768 ARINC-429 words for transmission on the DITS bus.

The data stored in memory can be updated "on the fly", i.e., while the 53A-425 Card is transmitting. Transmission data in each memory is organized into "frames" consisting of a header word, for frame control, and one or more ARINC-429 data words. The header word controls the time interval between the start of one frame and the start of the next frame, and whether data in memory is to be transmitted once or continuously. To allow frame-by-frame testing of word-format protocol, the header word also controls parity (odd/even), word length (31, 32, or 33 bits), and the interword gap (two or four bit times) for the frame's ARINC-429 data words. The bit rate for each channel is programmable from 122 b/s to 125 kb/s, or an external clock can be used to set the bit rate.

The 53A-425 Card has Direct Memory Access (DMA) transfer capability to efficiently accept data from the system controller. Using a system controller with DMA capability, the card supports memory updating "on the fly" when all four buses are operating at 100-kHz bit rates. Either a programmable frame-by-frame interrupt, or a readback of the address of the last ARINC word transmitted, allows the user to synchronize updates to the card with the actual data transmission.

The differential data output voltage levels may be programmed independently on each channel to ±13 V, ±10 V, ±6.5 V, or ±2.5 V, line-to-line, to allow high-level, standard-level, low-level, and no-data-level receiver parametric electrical testing.

Extensive self test capabilities are provided, including a wraparound check of each channel, self test of the PROM and RAM memories, and testing of the bit-rate and frame-rate counter/timers on the card. Error reporting provides readback of any errors encountered during self test or during programming. Status LEDs at the front edge of the card provide a visual indication of programming errors and data transmission on each channel.

## CONTROLS AND INDICATORS

The following controls and indicators are provided to select and display the functions of the 53A-425 Card's operating environment.

### Address-Select Switch

The 53A-425 Card has a miniature, 10-position switch labeled "ADDRESS" that selects the 53A-425 Card's address (0-9) in the 53/63 Series System. The switch's cover opens to allow the address to be reselected. A screwdriver with a narrow, flat blade should be used to turn the cam-action wiper to the desired address position.

### Power LED

The Power LED provides a valuable diagnostic tool by giving the system programmer a visual indication of the action which the system is currently taking. Whenever the 53A-425 Card is addressed by the system controller, the LED goes out. The LED remains out until another function card is addressed. Since only one function card can be addressed at a time, an unlit Power LED indicates the function card with which the system controller is currently communicating. The Power LED being lit not only indicates that the 53A-425 Card is unaddressed, but that all required dc power (5 V dc, ±15 V dc) is being supplied.

### Fuses

The 5-volt dc and ±15-volt dc power buses each have a fuse that protects the system from overloads. If any fuse has blown, the Power LED will not light.

### Function LEDS and Switches

#### LEDs

The following LEDs are provided at the top front edge of the 53A-425 Card to indicate the status of the card's operation:

#### Status LEDs

Five LEDs are located near the front-edge connector, arranged in the order listed below, which indicate the following:

| Status LED | Definition |
|---|---|
| XMIT1 | When lit, channel 1 is transmitting data over the Mark 33 DITS bus. |
| XMIT2 | When lit, channel 2 is transmitting data over the Mark 33 DITS bus. |
| XMIT3 | When lit, channel 3 is transmitting data over the Mark 33 DITS bus. |
| XMIT4 | When lit, channel 4 is transmitting data over the Mark 33 DITS bus. |

ERR

1. During self test, the ERR LED blinks on and off. If an error is encountered during self test, the ERR LED stays on continuously.

2. The ERR LED lights if a syntax error is encountered during programming. The LED will go out when the error is reported to the system controller.

Switches

The following switches are provided to select the proper functions for the 53A-425 Card's operating environment:

Halt Switch

This two-position slide switch is located near the card's backplane edge connector. It selects the state of the 53A-425 Card after an @XH (Halt) or STOP command is received by the 53/63 Series System.

a. If the Halt Switch is in the ON position, then the 53A-425 Card is reset to its power-up state, all parameters are reset to their default values, and the Power LED is lit.

b. If the Halt Switch is in the OFF position, then the 53A-425 Card becomes unaddressed, the Power LED is lit, and any programmed parameters of the card remain unchanged.

## SPECIFICATIONS

| | |
|---|---|
| Configuration: | Quad ARINC-429 Transmitter |
| Coupling: | Connects directly to Mark 33 DITS bus. |
| RAM: | 32K x 32 RAM memory associated with each channel for data and control instructions. |
| Processor: | Intel 80186 (LCC). |
| Error Buffer: | 16 errors, maximum. |
| Parity (programmable): | The 53A-425 Card can generate odd or even parity, programmable on a frame-by-frame basis for each channel. |
| DITS Word Format (programmable): | The transmitted DITS word can have 31, 32 or 33 bits, programmable on a frame-by-frame basis for each channel. |
| Interword Gap (programmable): | Between words: two or four bit times, programmable on a frame-by-frame basis for each channel. |
| Frame Interval (programmable): | Delay between the start of one frame and the start of the next frame: 5 ms to 4 s in 1-ms steps, programmable on a frame-by-frame basis for each channel. Delay accuracy: one bit-rate clock cycle ±150 us, one channel transmitting; one bit-rate clock cycle ±500 us, four channels operating. |
| Bit-Rate Period (programmable): | 8 $\mu$s to 8.19 ms in 250-ns steps, programmable independently for each channel. |
| Data-Transfer Rate: | 2 $\mu$s, maximum (time required by card to receive and store one byte of data into memory). |
| 53A/63A System Interrupts (programmable): | Programmable on a frame-by-frame basis for each channel to indicate the start of a frame. |
| ARINC Output (each channel) | |
| Type Output: | Differential. |
| Programmable Voltage Levels (no load to full load): | Normal Levels |

Logic High:
Line A to Ground - +5 ± 0.25 V.
Line A to B - +10 ± 0.50 V.
Line B to Ground - -5 ± 0.25 V.

Logic Low:
Line A to Ground - -5 ± 0.25 V.
Line A to B - -10 ± 0.50 V.
Line B to Ground - +5 ± 0.25 V.

Logic Null:
Line A to Ground - 0 ± 0.25 V.
Line A to B - 0 ± 0.50 V.
Line B to Ground - 0 ± 0.25 V.

Parametric High Levels

Logic High:
Line A to Ground - +6.5 ± 0.325 V.
Line A to B - +13.0 ± 0.650 V.
Line B to Ground - -6.5 ± 0.325 V.

Logic Low:
Line A to Ground - -6.5 ± 0.325 V.
Line A to B - -13.0 ± 0.650 V.
Line B to Ground - +6.5 ± 0.325 V.

Logic Null:
Line A to Ground - 0 ± 0.25 V.
Line A to B - 0 ± 0.50 V.
Line B to Ground - 0 ± 0.25 V.

Parametric Low Levels

Logic High:
Line A to Ground - +3.25 ± 0.163 V.
Line A to B - +6.50 ± 0.326 V.
Line B to Ground - -3.25 ± 0.163 V.

Logic Low:
Line A to Ground - -3.25 ± 0.163 V.
Line A to B - -6.50 ± 0.326 V.
Line B to Ground - +3.25 ± 0.163 V.

Logic Null:
Line A to Ground - 0 ± 0.25 V.
Line A to B - 0 ± 0.50 V.
Line B to Ground - 0 ± 0.25 V.

Parametric Null Levels

Logic High:
Line A to Ground - +1.25 ± 0.1 V.
Line A to B - +2.50 ± 0.2 V.
Line B to Ground - -1.25 ± 0.1 V.

Logic Low:
Line A to Ground - -1.25 ± 0.1 V.
Line A to B - -2.50 ± 0.2 V.
Line B to Ground - +1.25 ± 0.1 V.

Logic Null:
Line A to Ground - 0 ± 0.25 V.
Line A to B - 0 ± 0.50 V.
Line B to Ground - 0 ± 0.25 V.

Rise/Fall Time: 16 kb/s to 125 kb/s: 1.5 ± 0.5 μs.

0 b/s to 16 kb/s: 0 ± 5 μs.

Output Impedance: 75 ± 5 Ohm, balanced.

Drive Capability: 20 ARINC receivers (400-Ohm minimum load).

Auxiliary Inputs/Outputs (each channel)

Sync Out*:
Type output: TTL.
Drive: 6 standard TTL loads.
Sense: High while ARINC-429 word is being transmitted.

Frame Transmitting*:
Type output: TTL.
Drive: 6 standard TTL loads.
Sense: Low while frame is being transmitted.

Clock Out*:
Type output: TTL.
Drive: 6 standard TTL loads.
Sense: Free-running clock at ARINC-429 data-transmission bit rate.
Duty cycle: 50%.

NRZ Data Out*:
Type output: TTL.
Drive: 6 standard TTL loads.
Sense: ARINC-429 output data in NRZ, high-true format. Data is valid on the falling edge of Data Clock Out.
Transmission order: LSB of ARINC-429 word first.

Data Clock Out*:
Type output: TTL.
Drive: 6 standard TTL loads.
Sense: NRZ data is valid on the falling edge of Data Clock Out. One output pulse for each data bit transmitted.
Duty Cycle: 50%.
Rate: Equal to ARINC-429 bit rate.

External Clock Input:

Type input: TTL-compatible.
Loading: 0.8 standard TTL load.
Range: 0-Hz to 125-kHz square wave, 50% duty cycle.

*These signals are intended for use by the 53A-427 ARINC-429/561 Converter Card.

Power-Up:

The 53A-425 Card powers up to the following states:

- Interrupts disabled.
- 100-kb/s bit rate for all channels.
- Transmitter outputs in null state.
- Internal bit-rate clock selected.
- Channel 1 selected.
- Power LED lit.
- XMIT1 LED out.
- XMIT2 LED out.
- XMIT3 LED out.
- XMIT4 LED out.
- ERR LED out if no self-test errors are found.
- Channel-memory addresses at location 0.

Self Test Performed:

Memory, time-base, and output-data tests (data output wrapped around to one of the processor's input ports prior to differential drive amplifiers).

*NOTE:* During self test, test patterns are transmitted over DITS bus at parametric null voltage level (below user receiver threshold).

Power Requirements:

5V and ±15V dc power is provided by the internal Power Supply in the 53/63 Series Card Cage.

Voltage (5-volt Supply):

4.75 V dc to 5.25 V dc.

Current (5-volt Supply):

1.6 A, maximum quiescent.
1.7 A, peak.

Voltage (±15-volt Supplies):

+14.5 V dc to +15.5 V dc.
-14.5 V dc to -15.5 V dc.

Current (+15-volt Supply):

100 mA, maximum quiescent.
105 mA, peak.

Current (-15-volt Supply):

95 mA, maximum quiescent.
100 mA, peak.

Cooling:

Provided by fan in the 53/63 Card Cage.

| | |
|---|---|
| Temperature: | -10 °C to +65 °C, operating (assumes ambient temperature of 55 ° and airflow to assure less than 10 °C temperature rise).<br>-40 °C to +85 °C, storage. |
| Humidity: | Less than 95% R.H., noncondensing. |
| Dimensions: | 197 mm high, 221 mm deep, 13 mm wide.<br>(7.75 in x 8.69 in x 0.5 in). |
| Dimensions, Shipping: | When ordered with a 53/63 Card Cage, the card is installed in one of the card cage's function-card slots.<br><br>When ordered alone, the shipping dimensions are:<br><br>254 mm x 254 mm x 127 mm.<br>(10 in x 10 in x 5 in). |
| Weight: | 0.64 kg. (1.4 lb). |
| Weight, Shipping: | When ordered with a 53/63 Card Cage, the card is installed in one of the card cage's function-card slots.<br><br>When ordered alone, the shipping weight is:<br><br>1.00 kg. (2.2 lb). |
| Mounting Position: | Any orientation. |
| Mounting Location: | Installs in any function-card slot of the 53/63 Series Card Cage. |
| I/O Connection: | A 48-pin hooded connector (53A-780) connects to all front-edge signals. |
| Required Equipment (not supplied): | 53A-780 Hooded Connector, or 53A-746 Analog Cable (contain Channel 1-4 Line A and Line B signals only). |
| Equipment Supplied: | 1 - 53A-425 Quad ARINC-429 Transmitter Card.<br>1 - Spare fuse (Part #42202-52001).<br>1 - Spare fuse (Part #42202-52004).<br>1 - Operating Manual (Part #00000-14250).<br>1 - Service Manual (Part #00000-24250). |

## DATA-TRANSMISSION FORMAT

Data output to a channel on the 53A-425 Card is organized into frames. Each frame consists of a single header word followed by one or more ARINC data words. Each header word or ARINC data word is four bytes long. The most significant bit of the fourth byte of each word specifies whether the word is a header word or an ARINC data word. A bit value of 1 specifies a header word; a bit value of 0 specifies an ARINC data word. A channel can receive multiple frames, limited only by the channel's RAM size of 32K words.

In this manual, as in other 53/63 Series System manuals, "input" refers to data flow from the 53/63 Series System to the system controller (calculator or computer); "output" refers to data flow from the system controller to the 53/63 Series System.

### Header Word

The header word, which is output to an individual channel's memory as four 8-bit bytes, contains the control information listed below:

- The delay between the start of the current frame and the start of the next frame.
- Output transmission parity (odd or even).
- Output data-word length (31, 32 or 33 bits).
- Interword-gap time between data words in the current frame (two or four bit times).
- Whether to stop transmitting after the preceding frame's data has been transmitted, or to wrap around and continue transmitting from the top of memory.

*NOTE:* A frame with a header word, but no ARINC data words, is treated as if the frame contains data words, i.e., the frame time is still used as a delay time. The first word in a channel's memory must be a header word; otherwise, an error is returned, and the channel will not start transmitting.

Figure 425-1 shows the format of a header word.

First output byte:

| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Data | T3 | T2 | T1 | T0 | X | X | X | X |

Second output byte:

| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Data | T11 | T10 | T9 | T8 | T7 | T6 | T5 | T4 |

Third output byte:

| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Data | STOP | TMWRP | INT | X | IWG | LEN33 | LEN31 | EVNPAR |

Fourth output byte:

| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Data | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

X = Don't care.

A bit value of 1 means "high" or true.

A value of 1 in bit 7 of the fourth output byte means that this 4-byte word is a header word.

*Figure 425-1: Header-Word Format for the 53A-425 Card*

T0-T11

Bits T0 through T11 are the data for the frame's delay time. Each frame's delay time is the time between the start of that frame and the start of the next frame. Setting particular T bits true causes the sum of the delay times for those bits to become the frame's delay time.

| T Bit | Delay Time (ms) |
|---|---|
| 0 | 1 |
| 1 | 2 |
| 2 | 4 |
| 3 | 8 |
| 4 | 16 |
| 5 | 32 |
| 6 | 64 |
| 7 | 128 |
| 8 | 256 |
| 9 | 512 |
| 10 | 1024 |
| 11 | 2048 |

The maximum delay time which can be programmed (all T bits = 1) is 4.095 s; the minimum delay time is 5 ms. If a delay time of less than 5 ms is programmed for a frame, that frame's delay time automatically defaults to 5 ms.

*NOTE:* If the time required to transmit the ARINC data within a frame exceeds that frame's delay time, an error will be generated (error code Y6, Delay-time error), and transmission will cease on the affected channel.

STOP

If the STOP bit is set, the channel stops transmitting after the preceding frame has been transmitted. If the first header word in a channel's memory has the STOP bit set, the channel will not transmit, and interrupts will not be returned.

TMWRP

If the TMWRP (top-of-memory wrap) bit is set, the channel will continue transmitting from the top of memory. Data words following a header word whose TMWRP bit is set will be ignored.

INT

If the INT bit is set, then at the start of the current frame, a 53/63 Series System backplane interrupt is generated; this assumes that interrupts have been enabled previously with the I (Interrupt) command. For a discussion of 53/63 Series System backplane interrupts, see the @XS command in the 53A-171 Control Card Operating Manual. Depending on the type of communications card installed in the 53/63 Series System, a backplane interrupt will also generate an interrupt back to the system controller. In the case of a 53A-128 Communications Card, for example, a backplane interrupt generates an SRQ (service request) on the IEEE-488 bus.

IWG

IWG specifies the interword-gap time between the current frame's ARINC data words:

IWG = 0 specifies four bit times between words; this is the normal interword-gap time for an ARINC data word.

IWG = 1 specifies two bit times between words.

LEN33, LEN31

LEN33 and LEN31 specify the length of the current frame's ARINC data words:

| LEN33 | LEN31 | |
|---|---|---|
| 0 | 0 | 32-bit word selected. This is the length of a normal ARINC data word. |
| 0 | 1 | 31-bit word selected. |
| 1 | 0 | 33-bit word selected. |
| 1 | 1 | Illegal value. |

*NOTE:* When a 33-bit word is selected, bit 32 will be output as a 0, and bit 33 will be the parity bit. When a 31-bit word is selected, bit 31 will be the parity bit.

EVNPAR

EVNPAR specifies the parity of the current frame's ARINC data words:

EVNPAR = 0 specifies odd parity; this is the normal ARINC parity.

EVNPAR = 1 specifies even parity.

ARINC Data Word

Each 32-bit ARINC data word is stored as four 8-bit bytes. The order in which each byte is transmitted and the ARINC data bits contained in each byte are shown in Figures 425-2a and 425-2b.

---

First output byte:

| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ARINC Data Bits | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
| Label | Most significant bit to least significant bit | | | | | | | |

Second output byte:

| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ARINC Data Bits | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 |
| Least Sig. Data Byte | Most significant bit to least significant bit | | | | | | | |

*Figure 425-2a: Transmission Order for ARINC Data Words (Bytes 1 and 2)*

Third output byte:

| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ARINC Data Bits | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 |
| Mid Sig. Data Byte | Most significant bit to least significant bit | | | | | | | |

Fourth output byte:

| Bit Position | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| ARINC Data Bits | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 |
| Most Sig. Data Byte | Value = 0 | Most significant bit to least significant bit. | | | | | | |

*Figure 425-2b: Transmission Order for ARINC Data Words (Bytes 3 and 4)*

BITS 1 THROUGH 8

Bits 1 through 8 of an ARINC word are assigned as the word label by ARINC Specification 429.

BITS 31 THROUGH 9

Bits 31 through 9 of an ARINC word are assigned as data by ARINC Specification 429.

BIT 32

Bit 32 of an ARINC data word (bit 7 of the fourth output byte) must be set to 0 to indicate to the 53A-425 Card that this is an ARINC data word and not a header word. Bit 32 of the ARINC data word is assigned as the parity bit by ARINC Specification 429, but it is not necessary for the system controller to output a parity bit to the 53A-425 Card. The 53A-425 Card will generate the parity bit in the hardware; the generated parity bit is based on the parity defined in the frame's header word.

## ARINC-429 Bus Data Transmission Order

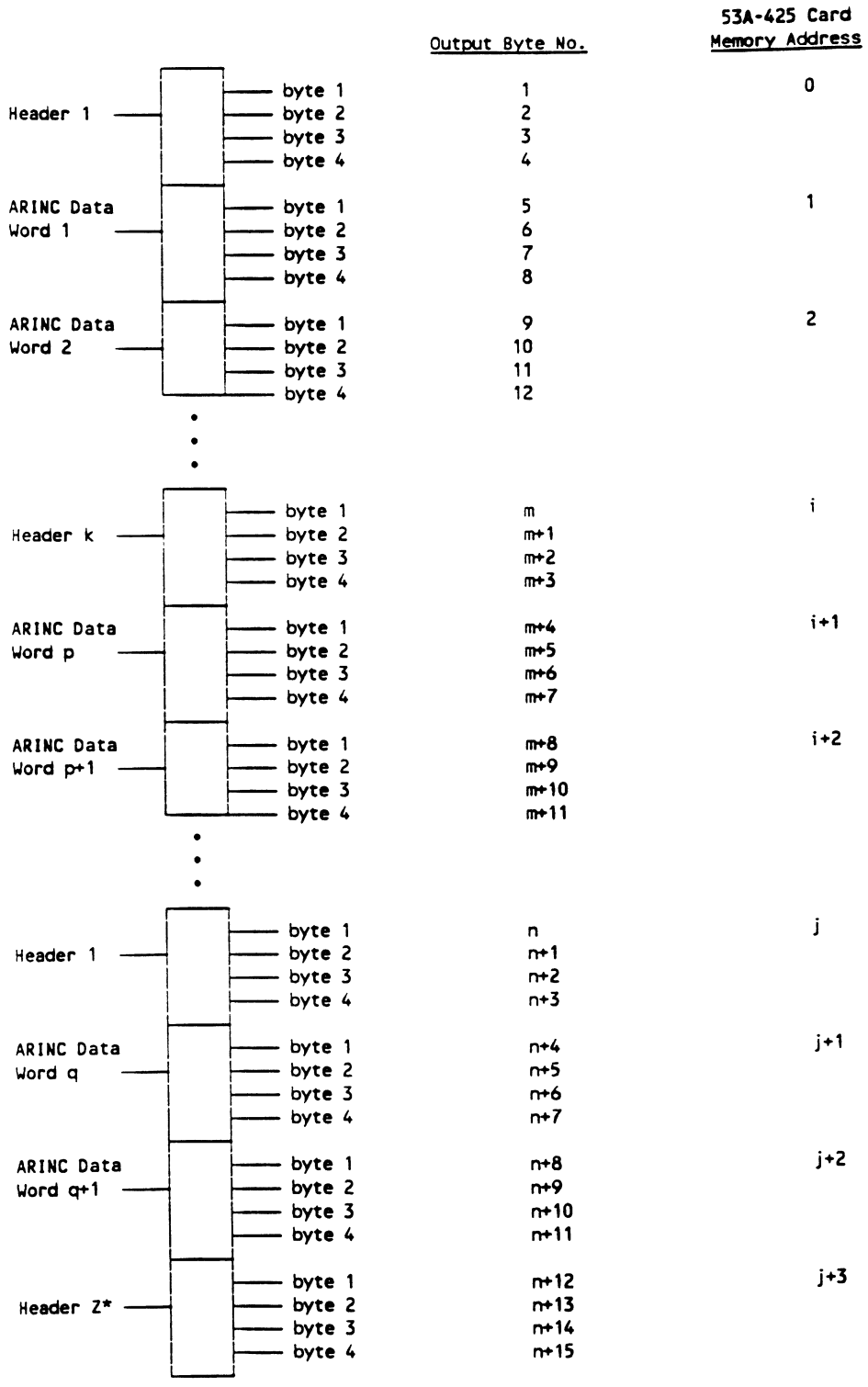
The order in which the system controller sends the ARINC data word's bytes to the 53A-425 Card and the order of the bits in each byte are based on the needs of the programmer and the requirements of ARINC Specification 429. The order in which data is transmitted on the ARINC-429 bus is ARINC data bit 1 first, bit 2 second, ..., and bit 32 last.

Looking at how the four output bytes are defined in Figures 425-2a and 425-2b above; bytes 1, 2, 3, and 4 are transmitted in that order. The most significant bit of byte 1, as output by the system controller, is transmitted first; the least significant bit of each of the other three bytes is transmitted first. This is because ARINC Specification 429 requires the order of transmission to be the label with the most significant bit first, followed by 24 bits of data with the least significant bit first.

The 53A-425 Card is designed to transmit the bits in the proper order, but to allow loading of the memory on the card with a label and data as they would be stored in the user's computer; i.e., the most significant bit of the label and of each data byte is the most significant bit as sent from the system controller to the card. This saves the programmer from having to write a routine to reverse the bit order of the label before it is sent to the 53A-425 Card.

## System Controller-to-Card Data Transmission Order

Data is sent to the 53A-425 Card in four 8-bit bytes as either a header word or an ARINC data word. The order in which the bytes are sent to the 53A-425 Card is shown in Figure 425-3.




*Header Z must be present, and either the STOP bit or the TMWRP bit must be set true. If Header Z is not present, the resulting operation is undefined.

*Figure 425-3: Order of Data Transmission from System Controller to Card*

"On-the-fly" Updates

Internal to the 53A-425 Card, ARINC-429 data words are moved from the main memory in 8-ARINC-word blocks to a separate, high-speed, 16-ARINC-word, FIFO memory prior to transmission on the DITS data bus. The ARINC data words and frame headers contained in main memory can be updated "on the fly" (while the 53A-425 Card is transmitting); these updates are limited by the following considerations:

1. Updates to the frame header currently being transmitted are not effective until the next pass through the transmission list.

2. Updates to the first eight ARINC data words of a frame that is within 5 ms of being transmitted are not sent on the bus until the next pass through the transmission list.

3. Updates to the next eight ARINC data words of the frame currently being transmitted are not sent on the bus until the next pass through the transmission list.

4. The header word following a frame whose last data word has already been transmitted cannot be changed to an ARINC data word.

When updating a channel's memory "on the fly", there are two ways of determining where the channel is in its transmission sequence:

1. Requesting input from the 53A-425 Card automatically provides the next memory address to be accessed by the selected channel; the address is always five ASCII digits with leading 0's. This feature is available at all times except when an error-code return is requested (see OPERATION section, E command).

2. The INT bit in the header can generate an interrupt to the system controller at the start of any user-selected frame.

# OPERATION

## Overview

The 53A-425 Card is programmed by ASCII characters issued from the system controller to the 53/63 System's communications card. The 53A-425 Card is interfaced to the communications card through the 53 Series or 63 Series Card Cage's backplane.

To address a function card for the first time, the system command @XY must be issued. X is the card cage address (0-9) selected on the 53A-171 Control Card in the addressed card cage; Y is the 53A-425 Card's address (0-9) within the addressed card cage. The 53A-425 Card's address is selected using the card's Address-select switch. Once a function card is addressed, it remains addressed until the system receives another @ character. Appendix A fully discusses the @XY command and the other 53/63 Series System commands. After the 53A-425 Card is addressed, individual card commands may be issued until another function card is addressed.

Actual programming of the 53A-425 Card is organized as follows:

One of the four ARINC-429 channels is selected for programming using the S (Select) command. After the S command is issued, all subsequent commands apply to the selected channel until another channel is selected.

R (Rate) and V (Voltage) commands are issued next in order to set the ARINC-429 data rate and output signal's voltage level.

An A (Address) command is issued next in order to define the starting address in the selected channel where header and ARINC-429 data words will be loaded. Following the A command, an L (Length) command is issued to inform the 53A-425 Card how many header and ARINC-429 data words are to be loaded into memory.

Header and ARINC-429 data words are then sent to the card, followed by a B (Begin) command to start ARINC-429 data transmission.

Additional card commands are available to stop data transmission (K and Q commands), restart data transmission (C command), enable or disable 53/63 Series System interrupts (I command), read back error status (E command), or retrieve contents of the user-loaded, on-card memory (M command).

Appendix D provides a sample BASIC program for loading and transmitting ARINC-429 data.

## Summary

An overview of the commands, listed alphabetically), is as follows:

A Address - sets an address in the selected channel's memory where the frame headers and ARINC data are to start being loaded, or the memory address from where the M (Memory) command is to start reading back message RAM.

B Begin - starts transmission on a single channel or on all four channels.

C Continue - continues transmission on a single channel after a STOP bit has been encountered in a header word.

E Error - prepares the 53A-425 Card to return programming or hardware error codes to the system controller on its next request for input from the card.

I Interrupt - enables or disables the generation of 53/63 Series System interrupts.

K Kill - stops transmitter operation, and returns the 53A-425 Card to its power-up state.

L Length - specifies the number of header or ARINC data words to be transferred to the selected channel's memory.

M Memory - used to retrieve data previously loaded into the selected channel's memory.

Q Quit - stops transmission on a single channel, or on all channels, after a maximum of 17 words is sent by each transmitter.

R Rate - specifies the period (in nanoseconds) of the bit-rate clock for the selected channel.

S Select - selects the active channel for future commands.

T Test - performs a functional self test of the complete 53A-425 Card.

V Voltage - specifies the output voltage level (normal, parametric high, parametric low, or parametric null) for the selected channel's transmitter.

Card Commands

Detailed descriptions of the 53A-425 Card's commands, in the same order as listed above, are as follows:

| Command | Description |
|---|---|
| [addr]A | The A (Address) command sets an address in the selected channel's memory where the frame headers and ARINC data are to start being loaded, or the memory address from where the M (Memory) command is to start reading back message RAM. The selected channel is the last channel specified by an S (Select) command.<br><br>The A command is required only at the beginning of a data transfer. The 53A-425 Card automatically increments the address after every word is transferred.<br><br>[addr] is a 1- to 5-digit decimal integer, from 0 to 32767, that specifies the current memory address for the selected channel. If [addr] is omitted, the address is set to 0 (first word in memory). A 53A-425 Card memory location is 32 bits wide and contains one complete header word or ARINC data word. |

*NOTE:* The first header word loaded and its associated ARINC data words must start at memory address 0, and be contiguous. If they are loaded into noncontiguous memory locations, the random data in the nonprogrammed locations will be transmitted on the ARINC-429 bus. A word is defined as 32 bits or four bytes. Data loading always begins with byte 1 of a word.

Examples:

1. 14000A programs the memory address of the selected channel to 14000.

2. For the example shown in Figure 425-3, the command 2A starts data loading with ARINC Data Word 2. Data following ARINC Data Word 2 are loaded into the next consecutive memory addresses.

| Command | Description |
|---|---|
| [chan]B | The B (Begin) command starts transmission on a single channel or on all four channels. |

[chan] is a 1-digit decimal integer that specifies the following:

| [chan] | Begin Transmission on Channel(s) |
|---|---|
| 0 | 1-4 |
| 1 | 1 |
| 2 | 2 |
| 3 | 3 |
| 4 | 4 |

If [chan] is omitted, transmission starts on all four channels. The B command has no effect on channels already transmitting.

Examples:

1. 4B starts transmission on channel 4.

2. 0B (or simply B) starts transmission on all four channels.

| Command | Description |
|---|---|

[chan]C — The C (Continue) command continues transmission on a single channel after a STOP bit has been encountered in a header word.

[chan] is a 1-digit decimal integer that specifies the following:

| [chan] | Continue Transmission on Channel |
|---|---|
| 1 | 1 |
| 2 | 2 |
| 3 | 3 |
| 4 | 4 |

If a C command is issued for a channel which has not encountered a STOP bit in a header word, the command has no effect on that channel.

Internal to the 53A-425 Card, data for each channel is moved from main memory in blocks of eight ARINC words to a separate, 16-ARINC-word, high-speed, First In/First Out (FIFO) memory which drives a given channel's DITS data bus. Once a channel has halted transmission due to encountering a header word's STOP bit, a C command should not be issued until the FIFO memory has emptied. To determine when to issue the C command, proceed as follows:

1. Select the desired channel using an S command, and request input from the card. The address of the current memory locations being processed will be returned.

2. When the returned current memory location is equal to the location of the header word containing the STOP bit, then wait for 576 times the programmed bit rate before issuing the C command.

| Command | Description |
|---|---|
| E | The E (Error) command prepares the 53A-425 Card to return programming or hardware error codes to the system controller on its next request for input from the card. Each returned error code consists of two ASCII characters followed by <CR><LF>. After an E command is initiated, the 53A-425 Card continues to return error codes on each input request from the system controller until 99 (no additional errors to report) is returned. Additional requests for input, after error code 99 is returned, cause the address of the last transmitted word from the last selected channel to be returned.<br><br>If an E command is issued and no errors are found, only error code 99 is returned. Because the error buffer can store a maximum of 16 errors, only the first 16 errors are returned; any additional errors are lost. Errors are returned in reverse order; i.e., the last error encountered is returned first, and the first error encountered is returned last.<br><br>See Appendix C for a list of returned error codes and error-code formats. |

| Command | Description |
|---|---|

[ena]I

The I (Interrupt) command enables or disables the generation of 53/63 Series System interrupts. The 53A-425 Card interrupts to indicate the start of transmission of a frame with the INT bit set in the frame's header word. After an interrupt occurs, it is latched by the 53A-425 Card, and will continue to generate a 53/63 Series System interrupt until the interrupt status of the 53/63 Series System is checked using the @XS command described in Appendix A.

[ena] is a 1-digit decimal integer that specifies the following:

| [ena] | Action |
|---|---|
| 0 | Interrupts are disabled. |
| 1 | Interrupts are enabled. |

Programming Caution:

When the applications program enters its interrupt handler and executes the @XS command, the handler should readdress the card cage immediately after receiving a colon (:). The following BASIC program illustrates one way to do this:

```
1000 REM INTERRUPT HANDLER
1010 PRINT "@1S"
1020 INPUT A$
1030 IF A$ = "1" GOTO 1100
1040 IF A$ <> ":" GOTO 1020
1050 PRINT "@1"
1060 RETURN
1100 REM 425 INTERRUPT HANDLER
      .
      .
      .
```

If the 53/63 Series System's card cage is not readdressed following the @XS command, subsequent interrupts from the 53A-425 Card may be lost.

| Command | Description |
|---|---|
| K | The K (Kill) command stops transmitter operation, and returns the 53A-425 Card to its power-up state. The ARINC transmitters immediately stop, regardless of how far the transmissions have progressed or how much data is in each transmitter's First In/First Out (FIFO) memory. This command also resets any errors and clears the Error LED. |

| Command | Description |
|---|---|
| [len]L | The L (Length) command specifies the number of header or ARINC data words to be transferred to the selected channel's memory. The selected channel is the last channel specified by an S (Select) command. |

[len] is a 1- to 5-digit decimal integer, from 1 to 32768, that specifies the number of header words and ARINC data words to be sent to the selected channel's message RAM.

After the L command is received, the 53A-425 Card sets the 53/63 Series System's backplane interface to the binary mode; all data output to the 53A-425 Card, after the L command, is treated as binary data and immediately stored in the selected channel's message RAM. Therefore, any <CR> and <LF> characters that might be sent by the system controller after the L command, as part of a "normal" output statement, must be suppressed; if they are not suppressed, they will be stored in message RAM as part of the channel's message data!

If an error is detected within the L command, the 53A-425 Card will purposely "hang up" the system controller. This is done to prevent binary data, following the L command, from being transmitted on the backplane and possibly being interpreted as ASCII data; e.g., binary 01000000 might be interpreted as the ASCII @ character, and cause another card to be addressed.

Example:

1000L sets the number of header and ARINC data words to be received by the selected channel to 1,000 words. Each of the 1,000 header or ARINC data words is sent by the system controller as four separate 8-bit bytes. The next character received, after the L character, is assumed to be a header or ARINC data word, and is stored in message RAM.

| Command | Description |
|---|---|
| [len]M | The M (Memory) command is used to retrieve data previously loaded into the selected channel's memory. The selected channel is the last channel specified by an S (Select) command. The command specifies the number of 4-byte words to be transferred from the selected channel's memory to the system controller. After issuing the M command, the 53A-425 Card expects the system controller to request four bytes of input for each of the number of words specified in the M command.<br><br>[len] is a 1- to 5-digit decimal integer, from 1 to 32768, that sets the number of 4-byte words to be transferred.<br><br>After the M command is received, the 53A-425 Card sets the 53/63 Series System's backplane interface to binary mode on each occurance of an input request. Any data output to the 53A-425 Card, after the M command is issued, will cause the card to terminate the M command. Therefore, any terminating <CR> or <LF> characters sent by the system controller after the M command, as part of a "normal" output statement, must be suppressed; if they are not suppressed, the 53A-425 Card will terminate the M command, and returned data will be the current transmission address of the selected channel.<br><br>If an error is detected within an M command, the 53A-425 Card will not complete the M command; the backplane will not go into binary mode, and all returned data will consist of the current transmission address of the selected channel.<br><br>Following the last 4-byte data word returned to the system controller, terminating <CR> and <LF> characters will be sent to the system controller by the card. |

| Command | Description |
|---|---|

[chan]Q

The Q (Quit) command stops transmission on a single channel, or on all channels, after a maximum of 17 words is sent by each transmitter. The Q command causes an asynchronous stopping of transmission at the end of a complete ARINC word, but in the middle of a frame. For a synchronous stopping of transmission at the end of a complete ARINC frame, the STOP bit should be set in a header word.

[chan] is a 1-digit decimal integer that specifies the following:

| [chan] | Channel(s) Stopped |
|---|---|
| 0 | 1-4 |
| 1 | 1 |
| 2 | 2 |
| 3 | 3 |
| 4 | 4 |

If [chan] is omitted, transmission stops on all four channels.

Internal to the 53A-425 Card, data for each channel is moved from main memory in blocks of eight ARINC words, to a separate, 16-ARINC-word, high-speed, FIFO memory which drives a given channel's DITS data bus. When a Q command is issued, the specified channel will not cease transmission until the FIFO memory associated with the channel has emptied. If a Q command is to be followed by a B command in order to restart transmission from the first word in memory, a time delay equal to 576 times the programmed bit rate should be placed between the issuance of the Q and B commands. Failure to do so will result in data transmission stopping in the middle of an ARINC word.

Examples:

1. 0Q stops transmission on all four channels.

2. 2Q stops transmission on channel 2.

| Command | Description |
|---|---|
| [per]R | The R (Rate) command specifies the period (in nanoseconds) of the bit-rate clock for the selected channel. The selected channel is the last channel specified by an S (Select) command. |

[per] is a 2- to 5-digit decimal integer, from 32 to 32767 (see Example 4 below for [per] = 00), that sets the bit-rate clock based on the following equation:

$$\text{bit-rate frequency (Hz)} = 1 / ([\text{per}] \cdot 10^{-9} \cdot 250)$$

The bit-rate clock for a given channel cannot be updated while the channel is transmitting; if this is attempted, no action is taken.

If there is an error in an R command and the selected channel is transmitting, no error is logged by the 53A-425 Card.

Examples:

1. 32R specifies a bit-rate frequency of 125 kHz (125 kb/s) for the selected channel.

2. 40R specifies a bit-rate frequency of 100 kHz (100 kb/s) for the selected channel.

3. 320R specifies a bit-rate frequency of 12.5 kHz (12.5 kb/s) for the selected channel.

4. The special case 00R (or simply R) sets the bit rate for the selected channel to the external bit-rate clock. Before issuing 00R, the transmitter's bit-rate clock should first be set to an internal bit rate that gives the proper rise and fall times according to the 53A-425 Card's specifications.

Command: F (Select Trigger Output)

Syntax: [chan][ftrg][VXItrg]F

Purpose: The F (Select Trigger Output) command specifies the front-panel and/or VXIbus TTL trigger line to be used as the output trigger line(s) for the specified channel(s).

Description:

[chan] a 1-digit decimal integer from 0 to 4 that specifies the channel(s) affected by the F command. Zero or no parameter specifies all channels.

[ftrg] a 1-digit decimal integer from 1 to 4 that specifies the front-panel trigger line to be used as the trigger output for the channel(s) defined by [chan].

| [ftrg] | Trigger line Selected |
|---|---|
| 1 | Front-panel Trigger 1 |
| 2 | Front-panel Trigger 2 |
| 3 | Front-panel Trigger 3 |
| 4 | Front-panel Trigger 4 |

If any other value other than those listed above are used for the [ftrg] parameter, the front-panel trigger lines will be disconnected from the channel(s) defined by [chan].

[VXItrg] a 1-digit decimal integer from zero to 6 that specifies the VXIbus TTL trigger line to be used as the trigger output for the channel(s) defined by [chan].

| [VXItrg] | Trigger line Selected |
|---|---|
| 0 | VXIbus TTL Trigger 0 |
| 1 | VXIbus TTL Trigger 1 |
| 2 | VXIbus TTL Trigger 2 |
| 3 | VXIbus TTL Trigger 3 |
| 4 | VXIbus TTL Trigger 4 |
| 5 | VXIbus TTL Trigger 5 |
| 6 | VXIbus TTL Trigger 6 |
| 7 | VXIbus TTL Trigger 7 |

If any other value other than those listed above are used for the [VXItrg] parameter, the VXIbus TTL trigger lines will be disconnected from the channel(s) defined by [chan].

Examples:

1. The command sequence 101F selects the VXIbus trigger line 1 as the output trigger line for channel 1 and disconnects all front panel trigger lines from channe 1.

2. The command sequence 011F (or 11F) selects the front-panel trigger line 1 and VXIbus TTL trigger line 1 as the output trigger lines for all channels.

Errors: A Syntax error will result if an out-of-range value is specified for [chan] or if the number of characters for the [chan], [ftrg], and [VXItrig] parameters exceed 3 characters.

If a Syntax error is generated when the command is received, the command will be ignored.

| Command | Description |
|---|---|
| T | The T (Test) command performs a functional self test of the complete 53A-425 Card. For each channel, message RAM is fully tested, the output transmitters are looped back to a processor input port and checked prior to the final differential drive amplifiers, and the channel counter/timers are tested. After this test is performed, all data stored in message RAM is lost, and the card returns to its power-up state. The error code for any errors found during self test can be read back using the E (Error) command. This test takes approximately 45 seconds to perform.<br><br>Any characters received by the 53A-425 Card, following the T command, will not be processed until self testing of the card is complete. To avoid appearing to "hang up" the system controller during the self test period, any terminating <CR> or <LF> characters "normally" output by the system controller, following the T command, should be suppressed. |

| Command | Description |
|---|---|
| [lev]V | The V (Voltage) command specifies the output voltage level (normal, parametric high, parametric low, or parametric null) for the selected channel's transmitter. The selected channel is the last channel specified by an S (Select) command. |

[lev] is a 1-digit decimal integer, from 0 to 3, that specifies the following:

| [lev] | Action |
|---|---|
| 0 | Normal ARINC-429 data levels |
| 1 | Parametric high |
| 2 | Parametric low |
| 3 | Parametric null |

The output voltage level cannot be updated while the 53A-425 Card is transmitting ARINC-429 data.

Normal ARINC-429 data levels and parametric high, low, and null data levels are defined in the SPECIFICATIONS section of this manual.

## INSTALLATION

The 53A-425 Card is a function card; therefore, it may be plugged into any blue card slot. Setting the Address Select switch defines the card's programming address. To avoid confusion, it is recommended that the slot number and the programming address be the same.

CAUTION:

To avoid plugging the card in backwards, observe the following:

a. Match the keyed slot on the card to the key in the backplane connector. The component side should be to the right for a 53 Series Chassis and to the top for a 63 Series Chassis.

b. There are two ejectors on the card. Make sure the ejector marked "53A-425" is at the top for a 53 Series Chassis and to the left for a 63 Series Chassis.

CAUTION:

The 53A-425 Card is a piece of electronic equipment and therefore has some susceptibility to electrostatic damage (ESD). ESD precautions must be taken whenever the module is handled.

## APPENDIX A

## 53/63 SERIES SYSTEM COMMANDS

| Command | Description |
|---|---|
| @XY | The @XY (Address) command addresses a function card in the 53/63 Series System.<br><br>@ is a delimiter used by the 53/63 Series System.<br><br>X is a card cage address (0-9) defined by the Address-select Switch on the 53A-171 Control Card in the addressed card cage.<br><br>Y is a function-card address (0-9) defined by the Address-select Switch on the function card. Once a card cage/function-card combination is addressed, it remains addressed until the 53/63 Series System detects a new @ character. |
| @XS | The @XS (Status) command provides the interrupt status of all function cards within the mainframe defined by X. The mainframe backplane interrupt status of all function cards in the addressed mainframe is latched into the 53A-171 Control Card when the @XS command is issued. The 53A-425 Card has interrupt capability that indicates, under program control, the start of selected frames. All function cards in all mainframes become unaddressed after the @XS command. The 53A-171 Control Card Operating Manual describes the @XS command in detail. |
| @XH | The @XH (Halt) command halts all function cards within the card cage defined by X. The command does not affect function cards in other card cages. How a function card reacts to the @XH command depends on the card. In all cases, an addressed function card (Power LED out) becomes unaddressed (Power LED lit).<br><br>On the 53A-425 Card, the position of the Halt Switch determines the @XH command's effect:<br>1. If the Halt Switch is in the ON position, the 53A-425 Card resets to its power-up state.<br>2. If the Halt Switch is in the OFF position, the 53A-425 Card is simply unaddressed. |
| STOP | The STOP command is not a string of ASCII characters. The command is hard-wired from the system controller (calculator or computer) to the 53/63 Series System communications card in each mainframe.<br><br>When the system controller issues a STOP command, each function card, including the 53A-425 Card, reacts as if it received the @XH command described above.<br><br>How the system controller executes the STOP command depends on the communications card used. With the 53A-128 IEEE-488 Card, for example, a STOP command is executed when the system controller asserts the IEEE-488 bus line IFC (Interface Clear) true. |

## APPENDIX B

## FRONT-EDGE-CONNECTOR PIN ASSIGNMENTS

| Pin No. | Function |
|---|---|
| 1 | CHANNEL 1 LINE A |
| 2 | CHANNEL 1 LINE B |
| 4 | CHANNEL 1 EXT CLK IN |
| 5 | CHANNEL 1 FRAME TRANSMITTING |
| 7 | CHANNEL 2 LINE A |
| 8 | CHANNEL 2 LINE B |
| 10 | CHANNEL 2 EXT CLK IN |
| 11 | CHANNEL 2 FRAME TRANSMITTING |
| 13 | CHANNEL 3 LINE A |
| 14 | CHANNEL 3 LINE B |
| 16 | CHANNEL 3 EXT CLK IN |
| 17 | CHANNEL 3 FRAME TRANSMITTING |
| 19 | CHANNEL 4 LINE A |
| 20 | CHANNEL 4 LINE B |
| 22 | CHANNEL 4 EXT CLK IN |
| 23 | CHANNEL 4 FRAME TRANSMITTING |
| 24 | GROUND |
| A | GROUND |
| B | CHANNEL 1 CLOCK OUT |
| C | CHANNEL 1 SYNC OUT |
| D | CHANNEL 1 NRZ DATA OUT |
| E | CHANNEL 1 DATA CLOCK OUT |
| F | GROUND |
| H | GROUND |
| J | CHANNEL 2 CLOCK OUT |
| K | CHANNEL 2 SYNC OUT |
| L | CHANNEL 2 NRZ DATA OUT |
| M | CHANNEL 2 DATA CLOCK OUT |
| N | GROUND |
| P | GROUND |
| R | CHANNEL 3 CLOCK OUT |
| S | CHANNEL 3 SYNC OUT |
| T | CHANNEL 3 NRZ DATA OUT |
| U | CHANNEL 3 DATA CLOCK OUT |
| V | GROUND |
| W | GROUND |
| X | CHANNEL 4 CLOCK OUT |
| Y | CHANNEL 4 SYNC OUT |
| Z | CHANNEL 4 NRZ DATA OUT |
| AA | CHANNEL 4 DATA CLOCK OUT |
| BB | GROUND |

A description of each of the front-edge-connector signals is given below:

CHANNEL n LINE A (pins 1, 7, 13, 19)

These are the analog output signals for direct connection to the ARINC-429 bus, line A.

CHANNEL n LINE B (pins 2, 8, 14, 20)

These are the analog output signals for direct connection to the ARINC-429 bus, line B.

CHANNEL n EXT CLK IN (pins 4, 10, 16, 22)

These signals let the user vary the bit rate for channel n on the ARINC-429 bus by supplying an external, TTL, clock signal. The external clock's frequency may vary between 0 Hz and 125 kHz. The duty cycle of the clock input must be 50% ± 2.5%.

CHANNEL n FRAME TRANSMITTING (pins 5, 11, 17, 23)

These outputs are TTL-level signals that indicate when a channel frame is actually being transmitted over the ARINC-429 bus. These signals go low at the beginning of a frame's transmission, and return high at the end of the frame's transmission.

CHANNEL n CLOCK OUT (pins B, J, R, X)

These TTL-level signals are free-running clocks at the ARINC-429 data-transmission bit rate and are intended for use with the 53A-427 ARINC-429/561 Converter Card as the XMIT Data Clock Inputs to the 53A-427 Card.

CHANNEL n SYNC OUT (pins C, K, S, Y)

These TTL-level signals go high at the beginning of each ARINC-429 word transmission and return low when the last bit of the ARINC word is transmitted. They are intended for use with the 53A-427 ARINC-429/561 Converter Card as the Sync Signal Inputs to the 53A-427 Card.

CHANNEL n NRZ DATA OUT (pins D, L, T, Z)

These TTL-level signals provide the ARINC-429 output data in NRZ, high-true format. Data on these lines is valid on the falling edge of Channel n Data Clock Out. The signals are intended for use with the 53A-427 ARINC-429/561 Converter Card as the DITS Word Inputs to the 53A-427 Card.

CHANNEL n DATA CLOCK OUT (pins E, M, U, AA)

These TTL-level signals provide clocks for strobing Channel n NRZ Data Out. A single output pulse occurs for each NRZ data bit. These signals are intended for use with the 53A-427 ARINC-429/561 Converter Card as the Data Clock Inputs to the 53A-427 Card.

In the above signal names, "n" represents a channel number (1 through 4). The pins noted in parentheses, following each signal name, correspond to channels 1 through 4, respectively.

# APPENDIX C

## ERROR CODES

Each error code is returned as two ASCII characters followed by <CR> and <LF> characters.

### Fatal Errors

Fatal errors cause the 53A-425 Card to disable the ARINC transmitter outputs. The 53A-425 Card will then accept commands from the system controller, but will not perform functions for any commands except the @XH command and the STOP command. Any input from the card will return only the error code for the fatal error.

| Error Code | | |
|---|---|---|
| Char 1 | Char 2 | Description |
| 0 | 0 | Message-RAM failure |
| 0 | 1 | Stack-RAM failure |
| 0 | 2 | Interrupt-controller failure |
| 0 | 3 | (Reserved) |
| 0 | 4 | General hardware failure |

### Nonfatal Errors

Nonfatal errors do not cause the 53A-425 Card to totally suspend its operations. However, a hardware error within a channel permanently disables transmission from that channel until the error is cleared.

| Error Code | | |
|---|---|---|
| Char 1 | Char 2 | Description |
| X | 0 | Unrecognized command |
| X | 1 | Invalid parameters (includes a value out of bounds) |

X = Number of channel selected when error occurred.

| Error Code | | |
|---|---|---|
| Char 1 | Char 2 | Description |
| Y | 2 | Frame-header error |
| Y | 3 | ARINC-transmitter error (hardware error) |
| Y | 4 | Time-base error (hardware error) |
| Y | 5 | Reserved |
| Y | 6 | Delay-time error (Frame's delay-time is too short) |
| 9 | 9 | No additional errors to report. |

Y = Number of channel in which error occurred

# APPENDIX D

## SAMPLE BASIC PROGRAM

## FOR LOADING AND TRANSMITTING ARINC-429 DATA

The sample program below is written in Advanced BASIC (BASICA) for an IBM PC. The PC is connected to the CDS card cage using a 53A-903 I/O Card installed in the PC. The 53A-903 I/O Card provides an IEEE-488 interface between the PC and the CDS card cage. The 53A-425 Card has been set to address 9. The address of the 53/63 Series System card cage containing the 53A-425 Card is address 1.

The sample program loads two frames of data into the 53A-425 Card. Each frame contains two identical ARINC-429 words. Following the second frame of data, a third header word is loaded to cause the 53A-425 Card to "wrap" back to the beginning of memory and continue transmission.

Line numbers 1000 through 1070 define the ARINC-429 header and data words to be sent to the 53A-425 Card at line 1080. The CALL statements at lines 1080 and 1100 transfer the contents of the string variable WRT$ to the 53A-425 Card.

Sample BASIC Program

In this program listing, lines which are not preceded by a line number (except for the one following 1070) are not part of the BASIC program. They are inserted here as comments to explain what the program is doing at each numbered line.

•
•
•

```
1000 HEADER$ = CHR$(0) + CHR$(192) + CHR$(0) + CHR$(128)
     HEADER$ is a 4-byte string used to define the frame's header word.
          Bytes 1 and 2 set the frame's delay time to 3.096 seconds.
          Byte 3 defines the following:
               - Stop bit is not set.
               - Top-of-memory wrap is not set.
               - Interrupt bit is not set.
               - Interword gap is set to 4 bit times.
               - Word length is set to 32 bits.
               - Parity is set to odd.
          Byte 4 defines this word as a header word.

1010 WHEADER$ = CHR$(0) + CHR$(0) + CHR$(64) + CHR$(128)
     WHEADER$ is a 4-byte string which defines a wrap-to-top-of-memory header word.
          Bytes 1 and 2 are ignored; they are not used in a wrap header word.
          Byte 3 defines the following:
               - Stop bit is not set.
               - Top-of-memory wrap is set.
               - Interrupt bit is not set.
               - Interword gap is not set; it is unused in a wrap header word.
```

- Word length is not set; it is unused in a wrap header word.
- Parity is not set; it is unused in a wrap header word.

Byte 4 defines this word as a header word.

```
1020 LABEL1 = 8
1030 LABEL2 = 37
1040 ARINCD1$ = CHR$(LABEL1) + CHR$(16) + CHR$(212) + CHR$(9)
1050 ARINCD2$ = CHR$(LABEL2) + CHR$(192) + CHR$(20) + CHR$(5)
```

ARINCD1$ and ARINCD2$ are 4-byte strings defining the ARINC data:

Byte 1 is the ARINC label; LABEL1 (distance to go) is for string variable ARINCD1$, and LABEL2 (time to go) is for string variable ARINCD2$.

Bytes 2, 3, and 4 are the ARINC data bytes. String variable ARINCD1$ contains a distance of 2750.4 nautical miles, and string variable ARINCD2$ contains a time of 145.3 minutes as taken from Attachment 6 of the ARINC-429 specification.

```
1060 C$ = "@191S40R0A7L"
```

C$ is a string used to define commands to be sent to the 53A-425 Card.

- @19 is the @XY address command.
- 1S sets the selected channel to 1.
- 40R sets the bit-rate frequency on the selected channel (channel 1) to 100 kHz (100 kb/s).
- 0A sets a 53A-425 Card memory address of 0 at which to start loading the header word and ARINC data words for the selected channel (channel 1).
- 7L sets the number of header and ARINC data words to be loaded to 7.

```
1070 WRT$ = C$ + HEADER$ + ARINCD1$ + ARINCD1$ + HEADER$ + ARINCD2$ +
       ARINCD2$ + WHEADER$
1080 CALL IBWRT(CDS%,WRT$)
```

Output the contents of string variable WRT$ to the 53A-425 Card.

```
1090 WRT$ = "1B"
```

Start transmission on channel 1.

```
1100 CALL IBWRT(CDS%,WRT$)
```

Output the contents of string variable WRT$ to the 53A-425 Card.

•
•
•